8.4: Current Temperature Stress Study of RF Sputter a-InGaZnO TFTs

Charlene Chen[1], Katsumi Abe[2], Hideya Kumomi[2], & Jerzy Kanicki[1*]
[1]Organic and Molecular Electronics Laboratory, Department of Electrical Engineering and Computer Science
The University of Michigan, Ann Arbor, Michigan 48109, USA
[2]Canon Research Center, Canon Inc., 30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo 146-8501, Japan
*Email: Kanicki@eecs.umich.edu

Abstract: *Current temperature stress (CTS) measurements were performed on RF sputter amorphous In-Ga-Zn-O (a-InGaZnO) thin film transistors (TFTs). We investigated the effect of stress current (I_{STR}) and stress temperature (T_{STR}) on the electrical properties of the a-InGaZnO TFTs when stressed in both the linear and saturation regimes.*

Keywords: current temperature stress (CTS); RF sputter; amorphous In-Ga-Zn-O (a-InGaZnO); thin film transistor (TFT); linear and saturation regime.

Introduction

Amorphous metal oxide (AMO) thin film transistors (TFTs) have recently emerged as a competitive technology for future active-matrix organic light emitting displays (AM-OLEDs) [1]. Besides visible transparency, decent mobility, sharp subthreshold slope, low off-current, low processing temperature, and high electrical uniformity over large area, many authors have also reported their electrical stability [2][3][4]. C. J. Kim et al. reported that the threshold voltage shift was ~0.2V for 100 hours of current temperature stress (CTS) for their InGaZnO TFTs [4]. T. Riedl et al. also reported that ZnO-SnO_2 TFTs with optimized composition exhibit threshold voltage shift of only ~0.3V after 1000 hours of bias temperature stress (BTS) [2][3]. In this paper, we performed current temperature stress (CTS) on RF sputter amorphous In-Ga-Zn-O (a-InGaZnO) TFTs, and for the first time, report on the effect of stress temperature (T_{STR}), stress current (I_{STR}) and TFT biasing condition on the device's electrical stability. This study is important to both the practical device application and fundamental understanding of the material properties.

Experimental

The TFTs were fabricated on glass substrates. The gate electrode Ti (5nm)/Au (40nm)/Ti (5nm) was deposited by electron-beam and patterned by lift off. The gate insulator SiO_2 (200nm) and a-InGaZnO thin film were both deposited by RF sputtering and patterned by wet etch. After annealing in air at 300°C for 20 min, the source/drain electrodes Ti (5nm)/Au (40nm)/Ti (5nm) were deposited by electron-beam and patterned by lift off. A SiO_2 film as the back channel protection layer (100nm) was deposited by RF sputtering and patterned by wet etch. Finally, the TFTs were annealed in air at 200°C for 1 hour [5]. Measurements were done in dark using a Hewlett-Packard 4156A semiconductor parameter analyzer. The device temperature was regulated by a heated chuck and a Signatone temperature controller with a precision of 0.1 K. Before each measurement, the TFTs were placed on the heated chuck which is set at the desired measurement temperature for 30min to allow for thermal equilibrium.

We used two different stress schemes for the CTS measurements: CTS_lin and CTS_sat [6]. CTS_lin and CTS_sat are equivalent to operating the TFT in the linear and saturation regime, respectively. For CTS_lin, during the stress mode, the gate was biased at 20V while a stress current (I_{STR}) was applied to the drain of the TFT, as shown in Fig. 1(a). The same TFT were stressed for a total stress time (t_{STR}) of 10000s, as illustrated in Fig. 2. At certain times (t_{STR} = 100s, 200s, 500s, 1000s, 2000s, 4000s, 6000s, 8000s, and 10000s), the stress mode was interrupted and switched to the sweep mode where a quick gate voltage sweep (V_{GS} = -5 →20V) was applied to measure the transfer characteristic in the saturation regime of operation (V_{DS} = 20V). For CTS_sat, during the stress mode, the gate and drain were externally shorted together, and I_{STR} was applied to the drain, setting the voltages at the gate/drain (V_{GS} = V_{DS}), as shown in Fig. 1(b). The total stress time and number of points when the stress mode was interrupted are the same as CTS_linear. In the sweep mode, the gate/drain voltages (V_{GS} = V_{DS}) were swept from -5 to 20V to measure the transfer characteristics in the saturation regime. The same measurement procedure described above was repeated for several levels of stress current (I_{STR}) and stress temperature (T_{STR}) for both CTS setups. Table 1 summarizes the CTS conditions used in this paper. For both CTS setups, after the 10000s CTS measurement, the TFT was annealed at 300°C for 1 hour to recover its initial characteristics, as shown in Fig. 3.

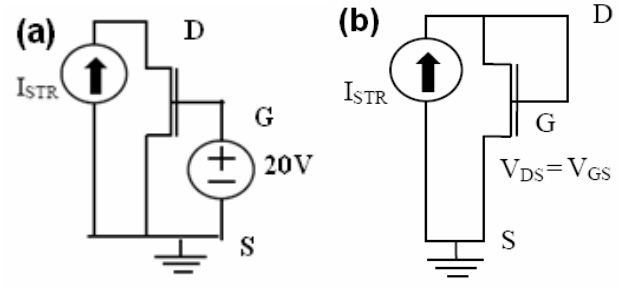

Figure 1. The two CTS measurement setups (stress mode) used in this study (a) CTS_lin (V_{GS} = 20V) and (b) CTS_sat (V_{GS} = V_{DS})

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Results

The initial (t_{STR} = 0) TFTs have field-effect mobilities of ~10cm^2/V-s, threshold voltages ~3V, current on-off ratios ~10^8, and subthreshold slopes in the order of ~0.4V/dec. The field-effect mobility and threshold voltage were extracted from linearly fitting $I_D^{1/2}$-V_{GS} measured in the sweep mode (fitting range V_{GS} = 5~20V). Fig. 4(a) shows an example of the TFT transfer characteristics measured during the sweep mode (V_{DS} = 20V, V_{GS} = -5 → 20V) of CTS_lin. The CTS_lin was performed at T_{STR} = 80°C with V_{GS} held at 20V, and I_{STR} = 10μA. For this level of stress current (I_{STR} = 10μA), the drain-to-source voltage (V_{DS}) of the TFT is measured to be around 0.6V, which indeed corresponds to the linear regime of operation. Fig. 4(b) shows an example of TFT transfer characteristics measured during the sweep mode (V_{DS} = V_{GS} = -5 → 20V) of CTS_sat. The CTS_sat was performed at T_{STR} = 80°C with the gate and drain tied together, and I_{STR} = 100μA, which sets V_{GS} = V_{DS} ~ 16.5V. As we can see from Fig. 4, even after suffering through these strict CTS conditions for 10^4sec, the TFT subthreshold slope and off-current remained almost the same, the field effect mobility slightly 10% decreases, and the threshold voltage only shifted ~2V for both CTS setups.

Table. 1 CTS conditions used in this paper

	Stress mode	Sweep mode	I_{STR}	T_{STR}
CTS_lin	$I_D = I_{STR}$ V_{GS} = 20V V_{DS}*	V_{GS} = -5→20V V_{DS} = 20V	10	40, 50, 60, 70, 80
			1, 10, 40, 100	60
CTS_sat	$I_D = I_{STR}$ $V_{DS} = V_{GS}$**	$V_{GS} = V_{DS}$ = -5→20	100	40, 50, 60, 70, 80
			40, 60, 80, 100	60

* V_{DS} increases with ΔV_T during the stress mode.
** V_{DS} = V_{GS} increases with ΔV_T during the stress mode.

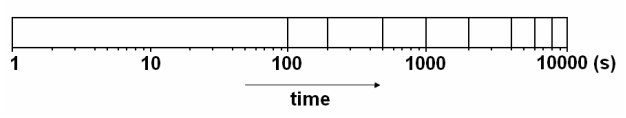

Figure 2. The CTS was performed on a single TFT for a total of 10000s. The white space indicates the stress mode, and the black lines indicate when the stress mode is interrupted and switched to the sweep mode.

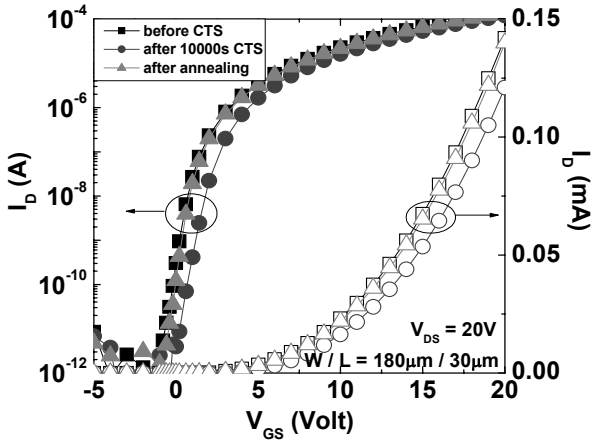

Figure 3. a-InGaZnO TFT transfer characteristics before CTS, after 10000s CTS, and after annealing at 300°C for 1 hour.

Stress Temperature Effect: We performed CTS measurements for both CTS setups at stress temperatures ranging from 40°C to 80°C. The stress currents are 10μA and 100μA for CTS_lin and CTS_sat, respectively. I_{STR} = 10μA is sufficient for the maximum drive current level of a 15" XGA full color AM-OLED (subpixel area A_{pix} ~30000μm^2), assuming a brightness (υ) of 1000 Cd/m^2 and an OLED efficiency (η) of 5Cd/A:

$$I_{OLED} = \frac{\upsilon \cdot A_{pix}}{\eta} \qquad (1)$$

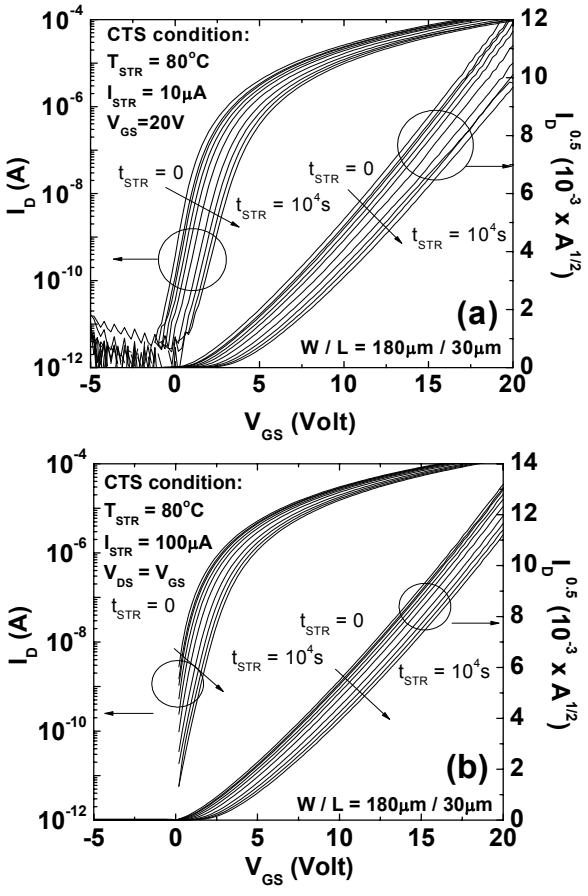

Figure 4. a-InGaZnO TFT transfer characteristics measured during the sweep mode of (a) CTS_lin and (b) CTS_sat.

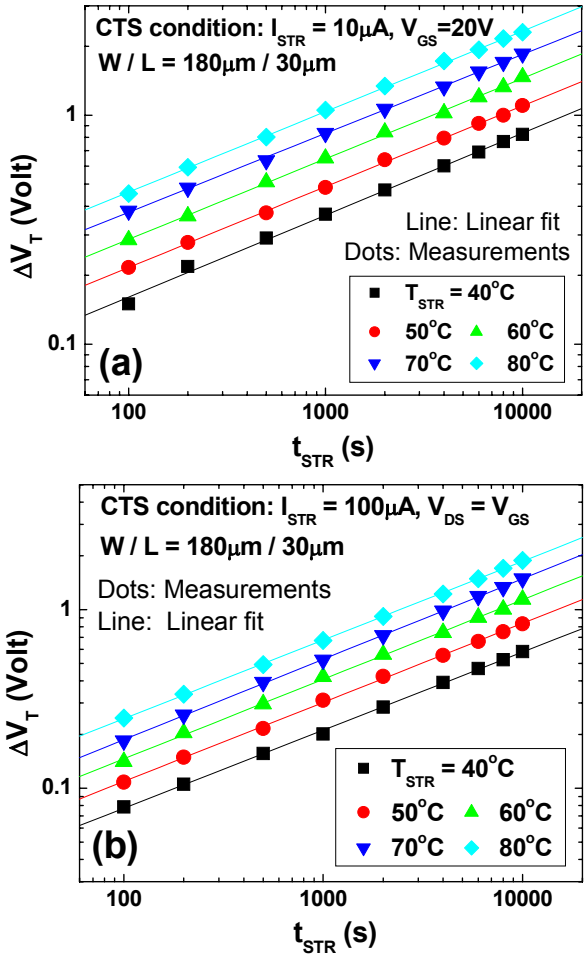

Figure 5. Threshold voltage shift (ΔV_T) as a function of stress time (t_{STR}) for various stress temperatures (T_{STR}) under (a) CTS_lin and (b) CTS_sat conditions.

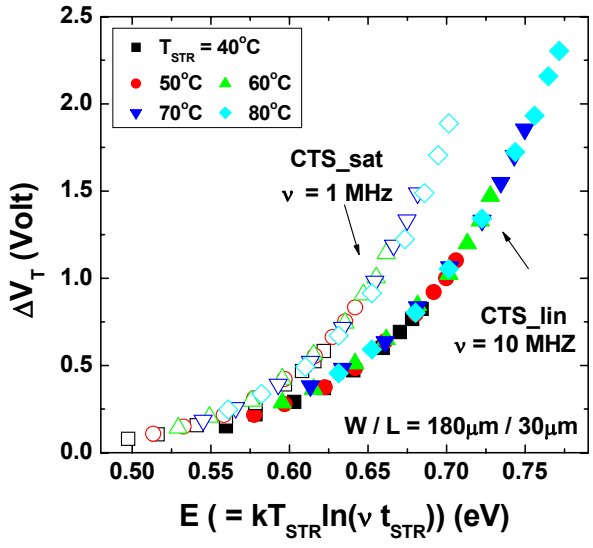

Figure 6. Threshold voltage shift (ΔV_T) as a function of thermalization energy (E). Unifying the effect of stress temperature (T_{STR}) and stress time (t_{STR}).

We used a much higher I_{STR} for CTS_sat to enhance the TFT parameter shifts, since from our experimental results, the TFTs are electrically more stable when stressed under CTS_sat compared to CTS_lin for the same I_{STR} level (see next section for further details). The device degradation is defined as the change in threshold voltage (V_T)

$$\Delta V_T = V_T(t = t_{STR}) - V_T(t = 0) \qquad (2)$$

V_T was extracted from linearly fitting $I_D^{1/2}$-V_{GS} measured in the sweep mode. The fitting range is chosen to be V_{GS} = 5~20V to avoid the effect of the subthreshold regime at smaller V_{GS} values. It should be noticed that the fitting range would affect the extracted V_T, due to the nonlinearity of the $I_D^{1/2}$-V_{GS} curve, and therefore should be carefully chosen. Fig. 5(a) and Fig. 5(b) show the TFT threshold voltage shift (ΔV_T) as a function of stress time (t_{STR}) for various T_{STR} under CTS_lin and CTS_sat, respectively. For both CTS setups, ΔV_T increases with T_{STR} for a given t_{STR}. We also observed that

$$\Delta V_T \propto t_{STR}^{\beta} \qquad (3)$$

for both CTS setups. β is extracted to be ~ 0.35 for CTS_lin, and ~ 0.45 for CTS_sat. We are not clear at this point if this discrepancy is related to the different CTS setups, or the inherent properties of the different TFT used. Also, we have not observed any temperature dependence of β in the investigated T_{STR} range so far.

A model that unifies the effect of stress temperature (T_{STR}) and stress time (t_{STR}) was developed for a-Si:H TFTs [7]. This model assumes a distribution of energy barriers $D(E_a)$ for defect (state) creation exist during bias stress: after a time t at a temperature kT all possible defect-creation sites with $E_a \leqq kT\ln(\nu t)$ will have converted into defects. The thermalization energy is therefore defined by

$$E = k \cdot T_{STR} \cdot \ln(\nu \cdot t_{STR}) \qquad (3)$$

where k is the Boltzmann constant and ν is the attempt-to-escape frequency. We investigated possible application of this thermalization energy concept to a-InGaZnO TFTs. By plotting ΔV_T as a function of E, a unique cure is obtained for both CTS setups with only one fitting parameter, the attempt to escape frequency ν, as can be seen from Fig. 6. The value of ν is 10^7 Hz for CTS_lin and 10^6 Hz for CTS_sat, and was determined to ensure the best overlap of the ΔV_T -E curves for all stress temperatures. Although the physical meaning of ν is unclear for our a-InGaZnO TFTs, eq. (3) describes very well our experimental data.

Stress Current Effect: We also performed CTS measurements at various I_{STR} levels. For CTS_lin, I_{STR} = 1μA, 10μA, 40μA, and 100μA, and for CTS_sat, I_{STR} = 40μA, 60μA, 80μA, and 100μA. Again, For CTS_sat, we didn't explore lower I_{STR} levels for the same reason mentioned previously. The stress temperature (T_{STR}) was fixed at 60°C. Fig. 6 shows the threshold voltage shift (ΔV_T) as a function of t_{STR} and injected charge Q_{inj} (=I_{STR} x t_{STR}) for various I_{STR} levels under CTS_lin

and CTS_sat. For CTS_lin, we can see that ΔV_T-t_{STR} (Fig. 6a) is almost independent of I_{STR}, while for CTS_sat, ΔV_T-t_{STR} increases with I_{STR} (Fig. 6b). On the other hand, when plotting ΔV_T-Q_{inj} of CTS_lin (Fig. 6c), for the same level of Q_{inj}, ΔV_T is more severe at lower I_{STR} levels due to the higher electrical field across the gate dielectric layer (E_{ox}) near the drain region, which is very different from CTS_sat, where E_{ox} near the drain region is held at zero for all levels of stress current, and ΔV_T is I_{STR} independent once normalized for Q_{inj} (Fig. 6d). The V_{GS} and V_{DS} values are summarized in Table I for both CTS setups and all I_{STR} levels. We conclude from our experimental results that for the same I_{STR}, the a-InGaZnO TFTs are electrically more stable when V_{GS} is smaller.

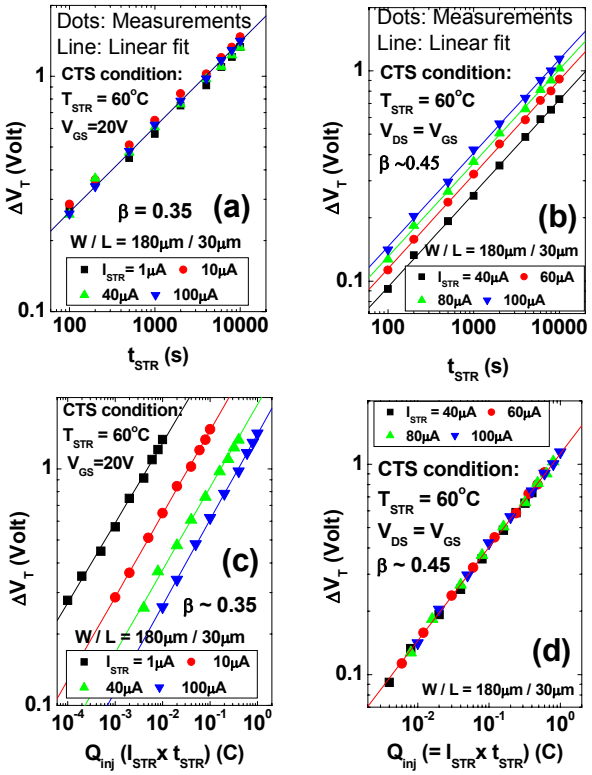

Figure 6. Threshold voltage shift (ΔV_T) as a function of stress time (t_{STR}) and injected charge (Q_{inj}) for various stress currents (I_{STR}) under (a)(c) CTS_lin and (b)(d) CTS_sat.

Table 1. V_{DS} and V_{GS} values for both CTS conditions.

CTS condition	I_{STR} (μA)	V_{DS}*(V) (t_{STR} = 0)
CTS_lin V_{GS} = 20V T_{STR} = 60°C	1	0.06
	10	0.56
	40	2.4
	100	7.5
CTS_sat V_{GS} = V_{DS} T_{STR} = 60°C	40	11.9 (=V_{GS})
	60	13.8 (=V_{GS})
	80	15.5 (=V_{GS})
	100	17.0 (=V_{GS})

* During CTS, V_{DS} increases with t_{STR}.

Conclusion

CTS measurements were performed on RF sputter a-InGaZnO TFTs. Several factors were considered when investigating the electrical stability of the devices, including the stress temperature, stress current, and biasing condition. We conclude that maintaining a smaller V_{GS} is beneficial to the TFT's stability, and for the same level of I_D, the TFTs are more stable when operating in the saturation regime then in the linear regime. The a-InGaZnO TFTs exhibit ΔV_T ~1V under 10000s stress with I_{STR} = 100μA, and T_{STR} = 60°C. The subthreshold slope, off-current, and field-effect mobility remain almost unchanged during the stress. Finally, both charge injection and electrical filed across the gate dielectric layer should be considered during CTS measurements.

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References

1. K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature,* vol. 432, pp. 488-492, 2004.

2. P. Görrn, P. Hölzer, T. Riedl, W. Kowalsky, J. Wang, T. Weimann, P. Hinze, and S. Kipp, "Stability of transparent zinc tin oxide transistors under bias stress ," *Appl. Phys. Lett,*. vol. 90, p. 063502, 2007.

3. T. Riedl, P. Görrn, P. Hölzer, and W. Kowalsky, "Ultra-high long-term stability of oxide-TTFTs under current stress," *Phys. Stat. Sol. (RRL),* vol. 1, no. 5, pp. 175-177, 2007.

4. C. J. Kim, D. Kang, I. Song, J. C. Park, H. Lim, S. Kim, E. Lee, R. Chung, J. C. Lee, and Y. Park, "Highly Stable Ga2O3-In2O3-ZnO TFT for Active-Matrix Organic Light-Emitting Diode Display Application," *IEDM 2006 Tech. Dig.,* 346769, 2006.

5. K. Abe, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, "Amorphous In-Ga-Zn-O based TFTs and circuits," *Int. Display Workshop*, AMD9-2, pp. 1779-1782, 2007.

6. A. Kuo, T. K. Won, and J. Kanicki, "Advanced amorphous silicon thin-Film transistors for AM-OLEDs: electrical performance and stability," *IEEE Tran. Electron Devices,* vol. 55, no. 7, pp. 1621-1629, 2007.

7. S. C. Deane, R. B. Wehrspohn, and M. J. Powell, "Unification of the time and temperature dependence of dangling-bond-defect creation and removal in amorphous-silicon thin-film transistors," *Physical Review B*, vol. 58, no. 19, pp. 12625-12628, 1999.